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10/775,523	02/09/2004	Sam Nemazic	SiliconStor-03US	1041

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EXAMINER

LEE, CHUN KUAN

ART UNIT	PAPER NUMBER
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2181

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/775,523	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 July 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>01/19/2007</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Currently, claims 1-20 are pending for examination.

2. Please note the arguments presented by the applicant on page 8, regarding the first task file and the second task file of the claimed invention, does not appear to be applicable to the independent claims 14 and 19, as each of the independent claims does not include the first task file in the first port and the second task file in the second port.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

5. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated January 19, 2007 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

IV. OBJECTIONS TO THE CLAIMS

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 14-20 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. The "first host task file", the "second host task file" and the "concurrent access the device through the switch, by acceptance of commands (e.g. non-data FIS), from either of the first or second host units, at any given time, including when the device is not in an idle state" are critical or essential to the practice of the invention, but not included in the claims is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

As disclosed by the applicant during the first interview for the application 10/775,488, on May 23, 2006, wherein the first interview is conducted for the clarification for the application 10/775,448 and the corresponding co-pending application, including the instant application (10/775523). The applicant disclosed the

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importance of "concurrency" associated with the enabling of the invention, wherein the "concurrency" is defined as the "acceptance of commands, from either of two or more hosts, at any given time including when a device (such as a storage unit) is not in an idle state," as demonstrated on Figure 6, showing the concurrent receiving of the commands from Host 1 and Host 2 are being stored in the Command Layer's Task File that is located in Fig. 6, ref. 310 and Fig. 6, ref. 320 and connected to the Host 1 and Host 2 respectively.

During the second interview, on October 06, 2006, the applicant further clarified that the implementation of receiving commands from either host 1 or host 2 "at any given time" is implemented by having a buffer for each corresponding hosts, such as the Command Layer's Task Files, therefore able to implement the claimed limitation of receiving commands from either host 1 or host 2 "at any given time," even before logging in of the host.

It appears that independent claims 14 and 19 does not include the claim limitations "first host task file" and "second host task file;" furthermore, independent claim 19 does not include the claimed limitation for the "concurrent access the device through the switch, by acceptance of commands (e.g. non-data FIS), from either of the first or second host units, at any given time, including when the device is not in an idle state."

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

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7. Claims 14-20 are rejected under 35 U.S.C. 112, second paragraph, as failing to set forth the subject matter which applicant(s) regard as their invention. Evidence that claims 14-20 fail to correspond in scope with that which applicant(s) regard as the invention can be found in the Interview Summary filed on May 23, 2006 and October 06, 2006. Please view the reasoning as stated above associated with the importance for the instant application regarding the "first host task file", the "second host task file" and the "concurrent access the device through the switch, by acceptance of commands (e.g. non-data FIS), from either of the first or second host units, at any given time, including when the device is not in an idle state," as disclosed by the applicant during the first and second interview.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. Claims 1-7 and 9-20 are rejected under 35 U.S.C. 103(a) as being anticipated by Grieff et al. (US Patent 6,961,813) in view of Utsunomiya et al. (US Pub.: 2003/0131166).

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9. As per claims 1, 9 and 14, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) links, for routing frame information there between the first and the second host units and the device, said switch comprising:

- a. a first SATA port (H0_Link Layer 130 of Fig. 1), responsive to a non-data frame information structure (FIS) and coupled to a first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- b. a second SATA port (H1_Link Layer 132 of Fig. 1), responsive to a non-data FIS and coupled to a second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- c. a third SATA port (Device-Side Link Layer of Fig. 1), responsive to a non-data FIS, coupled to a device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- d. an arbitration and control circuit (switch 110 and arbiter module 112 of Fig. 1) for selecting one of the first host or second host units to be coupled to the device, through the switch, and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27);

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wherein the switch enable multiple host units to share access to the device (e.g. single ATA device) (col. 3, ll. 14-16), such that the device can maintain communication with the multiple host units (col. 3, ll. 43-45); and

wherein the switch includes a buffer that allows the first host to post a single, non-queue command if the second host currently has outstanding queued commands (col. 5, ll. 36-39).

Grieff does not expressly teach the switch coupled between the plurality of host units and the device via SATA links, for routing frame information there between the first and the second host units and the device, said switch comprising:

wherein the first SATA port includes a first host task file;

wherein the second SATA port includes a second host task file;

selecting one of the first host or the second host units to concurrently access the device by accepting non-data FIS, from either of the first or the second host units, at any given time, including when the device is not in an idle state; and

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the non-data FIS to the switch for routing to the device.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file queue into Grieff's ATA ports. The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the second host unit; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands (i.e. non-data FIS), issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first

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task file queue and the second task file queue; therefore, as one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the command (i.e. non-data FIS) to the switch, stored by the respective task file queue, for routing to the device apparatus.

Therefore, it would have been obvious to combine Utsunomiya with Grieff for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]).

10. As per claims 2, 11 and 16, Grieff and Utsunomiya teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said device is a storage unit (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

11. As per claims 3, 12 and 17, Grieff and Utsunomiya teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

12. As per claims 4, 13 and 18, Grieff and Utsunomiya teach all the limitations of claims 1, 9 and 14 as discussed above, where Utsunomiya further teaches said switch comprising wherein said arbitration and control causes concurrent access of the device by the first and the second host units (Utsunomiya, Fig. 4-5).

13. As per claim 5, Grieff and Utsunomiya teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein a bit is used to indicate which host is the origin or destination of the non-data FIS (Grieff, col. 4, ll. 47-57 and col. 10, l. 27 to col. 12, l. 29), as each non-data FIS comprise an associated 5-bit tag utilized for identifying which host is the origin or the destination of the FIS.

14. As per claim 6, Grieff and Utsunomiya teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein said first, second and third ports are layer 2 ports (link layer ports) (Grieff, Fig. 1).

15. As per claims 7 and 10, Grieff and Utsunomiya teach all the limitations of claims 1 and 9 as discussed above, where Grieff further teaches said switch comprising wherein the switch provides for 'route aware' routing (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56 and col. 12, l. 60 to col. 14, l. 21), as FIS are properly routed between one of the associated hosts and the device.

16. As per claim 15, Grieff and Utsunomiya teach all the limitations of claim 14 as discussed above, where Grieff further teaches said switch comprising wherein the switch is a serial ATA switch (Grieff, col. 5, ll. 17-21).

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17. As per claim 19, Grieff teaches a method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween, comprising:

- a. receiving a non-data frame information structure (FIS) through a first serial ATA (SATA) port (H0_Link Layer 130 of Fig. 1), from to a first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- b. receiving a non-data FIS, through a second SATA port (H1_Link Layer 132 of Fig. 1), from a second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- c. receiving a non-data FIS through a third SATA port (Disk-Side Link Layer of Fig 1) (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- d. arbitrating (arbitrate utilizing the arbiter module 112 of Fig. 1) between the first and second host units and the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends request for execution by the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);
- f. coupling the device to the selected one of the first or second host units (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56); and

the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27).

Grieff does not teach the method for communication between multiple host units and the device comprising:

while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device.

Utsunomiya teaches a system and a method comprising:

a host computer issuing a plurality of commands to the drive apparatus (Fig. 3, ref. 12) at the same time (e.g. concurrently), wherein the drive apparatus operates in accordance to ATA ([0004] and [0007]);

a command queue including a task file queue enabling the host computer to issue the plurality of commands to be processed by the drive apparatus at the same time (e.g. concurrently), as the task file queue storing the plurality of commands ([0005]-[0008] and [0020]-[0024]), therefore the task file queue would enable the host computer to issue the plurality of commands, at any given time, even when the drive apparatus is in a busy status ([0005]); and

wherein the plurality of commands issued by the host computer are transferred from the task file queue to the drive apparatus' task file (Fig. 5 and [0022]).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Utsunomiya's task file queue into Grieff's ATA ports. The resulting combination of the references further teaches the switch comprising:

wherein the first SATA port includes the first task file queue (i.e. first host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the first host unit;

wherein the second SATA port includes the second task file queue (i.e. second host task file) storing the plurality of commands (i.e. non-data FIS) issued and sent by the second host unit;

wherein the switch selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device; and

wherein the switch selects either the first host unit or the second host unit to concurrently access the drive apparatus (i.e. device) as the switch receives and accepts the plurality of commands (i.e. non-data FIS), issued by either the first host unit or the second host unit, at any give time, including when the device is in the busy status (i.e. not in an idle state), as the plurality of commands are respectively stored into the first task file queue and the second task file queue; therefore, while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the command (i.e. non-data FIS) to the switch, stored by the respective task file queue, for routing to the device apparatus.

Therefore, it would have been obvious to combine Utsunomiya with Grieff for the benefit of decreasing the work load of the host unit for issuing commands (Utsunomiya, [0009]).

18. As per claim 20, Grieff and Utsunomiya teach all the limitations of claim 19 as discussed above, where Grieff further teaches the method comprising wherein the steps of transmitting a non-data FIS through the first SATA port, through the second SATA port, and transmitting a non-data FIS through the third SATA port (Grieff, col. 4, ll. 5-34 and col. 10, l. 27 to col. 12, l. 29), wherein the non-data FIS is transmitted from the host-side through either the first or the second serial ATA ports and from the device through the third serial ATA port.

19. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) and Utsunomiya et al. (US Pub.: 2003/0131166), and further in view of Kreifels (US Patent 4,891,788).

Grieff and Utsunomiya teach all the limitations of claim 1 as discussed above.

Grieff and Utsunomiya does not expressly teach said switch comprising a dual ported first-in-first-out (FIFO).

Kreifels teaches a system and a method comprising a dual port FIFO (Fig. 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels' dual port FIFO into Grieff and Utsunomiya's

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switch's inbound buffers. The resulting combination of the references teaches the switch further comprising the utilization of dual port FIFO.

Therefore, it would have been obvious to combine Kreifels with Grieff and Utsunomiya for the benefit of enabling the read and write operation of the inbound buffer to be independent of each other (Kreifels, col. 1, l. 15 to col. 2, l. 6).

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-20 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

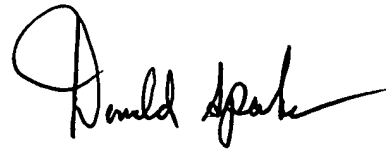
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 12, 2007

Chun-Kuan (Mike) Lee
Examiner
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A handwritten signature in black ink, appearing to read "Donald Sparks", with a stylized, flowing script.

DONALD SPARKS
SUPERVISORY PATENT EXAMINER